REMARKS

SUMMARY

In the Office Action dated March 25, 2004, the drawings were objected to because the first interface limitation from claim 1 was not explicitly shown as required by 37 CFR § 1.83(a). Furthermore, claims 1-3, 5-12, 15, 16, and 20 were rejected under 35 U.S.C. §112, 35 U.S.C § 102(b), and/or 35 U.S.C. §103(a). Additionally, claim 4, 13-14, and 17-19 were objected to as being dependent upon a rejected base claim.

The applicant has amended claims 1, 4, 6, 13, 17, and 20, canceled claims 11 and 12, and added new claims 21-26. Accordingly, claims 1-10 and 13-26 are currently pending. No new matter has been entered. Reconsideration of the pending claims is respectfully requested in light of these amendments and following remarks.

IN THE DRAWINGS

The examiner objected to the drawings because the first interface limitation from claim 1 was not explicitly shown as required by 37 CFR § 1.83(a). The applicant submits that the first and second interfaces are inherently shown in at least Fig. 2. Nonetheless, to expedite examination, the applicant has submitted herewith a replacement drawing sheet of Figure 2 illustrating a first host interface and a second IC interface in accordance with at least one embodiment. In particular, the applicant has included the word "(FIRST)" between "HOST" and "INTERFACE." Additionally, "(SECOND)" was added between "IC" and "INTERFACE" for purposes of clarity.

Additionally, the applicant submits herewith replacement drawing sheets for Figures 3-5. In the replacement drawing sheet illustrating Figure 3, the applicant has provided a reference to delay circuitry 109A/109B. In the replacement drawing sheet illustrating Figure 5, the applicant has provided a reference to R/W control signals 124. No new matter has been added.

IN THE SPECIFICATION

The applicant has amended the specification in four places to provide better clarity in the disclosure.

1) The terms "logic 112" was added after "write cycle decode" to help define this element.
2) The terms "data is" replaced "addresses are," and "address" replaced "data" respectively to clarify the function of these connections.
3) The identifier "130" relating to a mode control signal was replaced with "130a" to be consistent with the labels on the drawing sheets in two places.
4) The terms "first" and "second" were replaced with "third" and "fourth" respectively to improve the clarity of the disclosure.
No new matter has been added.

IN THE CLAIMS

Rejections to claims 1-6 under 35 U.S.C. §112, ¶2

In the Office Action dated March 25, 2004, claims 1-6 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

Claim 1 has been amended to include a comma after "first processor" to clearly communicate that the first interface can be connected to a first bus of a first processor, or a first and second bus of a second processor. The form of the claim is similar to a "Markush" style claim (an interchangeable one of x *and* y) as allowed by MPEP §2173.05(h). Thus, the applicant submits that with this amendment, claim 1 particularly points out and distinctly claims the subject matter which the applicant regards as the invention.

Claims 2-5 were also rejected as being dependent on claim 1. However, with the correction to the language of claim 1, the applicant submits claims 2-5 are in compliance with §112, ¶2.

Claim 6 was additionally rejected under § 112, ¶2. It appears that a misspelling appearing in claim 6 inadvertently created confusion. Claim 6 has now been amended to replace "on" with "one." As such, the applicant submits claims 6 is in proper form under § 112, ¶2.

Accordingly, the applicant requests that the rejection to claims 1-6 under 35 U.S.C. §112, ¶2 be removed.

Rejections to claims 11, 12, and 20 under 35 U.S.C. §102(b)

Claims 11, 12, and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by US Patent No. 4,967,346 issued to Freidin ("Freidin").

Claims 11 and 12 have been canceled without prejudice thereby rendering the rejections to claims 11 and 12 as moot.

As amended, claim 20 is directed to a processor, and recites (in part):

> ...
> interface logic to selectively couple said processor to an interchangeable one of a plurality of host processors, by providing a first interface for connection to a first bus of a first host processor having a first architecture type, or a first and second bus of a second host processor having a second architecture type to provide a selected one of said first and second host processors with access to said resources.

Thus, claim 20 recites interface logic that provides a first interface for connection to a first bus of a first host processor having a first architecture type, ***or*** a first and second bus of a second host processor having a second architecture type. In contrast, Freidin merely discusses read/write control signals and how they are created depending upon which type of processor is connected. The control signal connection scheme taught by Freidin cannot read on the bus interface elements of amended claim 20 because it only discloses a connection scheme for the control signals from multiple processor types and does not teach or otherwise suggest a method of connection with the address/data buses of multiple processor types. Thus, with the amended addition of the bus interface connection and for at least the reasons mentioned above, the applicant submits that claim 20 can not be anticipated by Freidin under § 102(b). As such, claim 20 should be in proper form for allowance and the applicant requests that the rejection be removed.

Rejections to claims 1-3, 5-10, 15, and 16 under 35 U.S.C. §103(a)

Claims 1-3, 5-10, 15, and 16 were rejected under 35 U.S.C. §103(a) as being obvious over Freidin in view of US Patent No. 5,740,466 issued to Geldman, et al. ("Geldman").

The subject Office Action states that Freidin shows a control interface capable of utilizing the read/write input control signals from either of two types of processors (an Intel type and a Motorola type), but does not show how the address/data buses could interface. The Office Action further states that Geldman teaches that certain Intel processors utilize a multiplexed address/data bus while certain Motorola processors use non-multiplexed address and data buses. According to the examiner, these two teachings imply that in order for Freidin's interface to operate it needs to not only properly handle the control signals, but also needs to route either the multiplexed address/data bus of one processor type or non-multiplexed buses of the other processor type to the device to make it fully compatible with either type of processor. *See* Office Action p. 5. The applicant, however, respectfully disagrees with this analysis.

The applicant's amended claim 1 as provided below is intended to be representative of claims 7 and 15. Claim 1 is directed to an integrated circuit and recites:

> switching logic; and
> a control interface having:
> a first interface for connection to an interchangeable one of a first bus of a first processor, or a first and second bus of a second processor,
> a second interface for connection to a data bus and an address bus of said switching logic, and
> selection logic coupled to said first and second interfaces and equipped to receive a control signal identifying one of a first control mode to couple said first bus of said first processor to both said data bus and said address bus of said switching logic, and a second control mode to couple said first bus of said second processor to said data bus of said switching logic and to couple said second bus of said second processor to said address bus of said switching logic.

While Freidin may disclose a simple interface circuit to automatically detect which type of processor is connected and reconfigure a 'type' flip-flop within the interface circuit to expect either a read & write strobe, or a data strobe & a read/write indicator, Freidin does not teach or otherwise suggest the different processor bus interface system as recited in at least claims 1, 7 and 15. In particular, Freidin does not teach or otherwise suggest a control interface having a first interface for connection to an interchangeable one of a first bus of a first processor, and a first and second bus of a second processor.

In fact, the applicant submits that Freidin teaches away from any implication of such an arrangement. For example, in its Background section Freidin states with respect to the Motorola "Motel" interface, ***a disadvantage*** is that although it allows either microprocessor type to be connected to a "part", such interface requires a 3-wire interconnection (*see* e.g. col. 1, lns. 35-40). Furthermore, Freidin states in the Summary Of The Invention section that interface circuitry is provided which allows an Intel or Motorola-type microprocessor ***to be connected via 2 wires*** (see e.g. col. 1, lns 46-50). Moreover, Freidin states that ***only a single data bus*** is used to transfer data after the control signals from the different processors are resolved. (*See* e.g. col. 2, lns. 15-23).

Furthermore, Freidin does not require the claimed processor data/address bus interface in order to function properly. For example, the device (12) that is connected to the processors (10,14) in Freidin's arrangement may have separate address/data bus connector ports for each type of processor. These address/data bus connector ports could then be coupled to a given device using additional glue logic not required by the applicant's invention as claimed. The control signal terminals of Freidin would still universally output read and write signals regardless of the connected processor type. Thus, the applicant submits that the mere fact that Freidin teaches a control signal interface having multiple bus interface methods, does not imply that Freidin's interface requires the applicant's claimed bus interface to properly function.

Geldman was cited for teaching that certain Intel processors utilize a multiplexed address/data bus while certain Motorola processors use non-multiplexed address and data buses. The applicant submits that although Geldman states that "the local

processor to controller communication path can be either a multiplexed address and data bus or a non-multiplexed address and data bus" (*see* e.g. col. 4, lns 35-41), Geldman nonetheless does not teach the address/data bus interface as recited in the applicant's claims 1, 7 and 15. More specifically, unlike Geldman's SCSI disk drive controller that is configured to work with a certain type of processor, the applicant's invention as claimed utilizes a unique address/bus interface system that interchangeably connects to both types of processors and can utilize the information being streamed on these buses regardless of the type of corresponding processor. Furthermore, while Geldman is directed to disk drive controllers that may need an initial setup change to select between the type of processor it will be operating with over a long period of time, the current inventive idea can be used in network switching devices that may need to rapidly accommodate a variety of different processor types. Thus, although Geldman mentions in passing that "the processor to controller communication path can interface to commercially available microprocessors...", Geldman does not teach the glueless address/data bus interface system as claimed in at least claim.

Although the applicant believes the above arguments sufficiently rebut the § 103 rejections, the applicant also asserts that there is no suggestion in either reference to combine these two pieces of prior art. As MPEP § 2143.01 states, "the mere face that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." Further, "the level of skill in the art cannot be relied upon to provide the suggestion to combine references." Here, neither reference contains a suggestion or motivation explicitly or implicitly to be combined, and neither the nature of the problem to be solved, the prior art teachings, nor the knowledge of an ordinary skilled artisan provides such a suggestion or motivation.

First, the applicant's invention as claimed provides a glueless processor interface having application in the network switch space. In solving this problem, the applicant addresses both the control signal interface and the address/data bus interface, thus providing a complete glueless interface. Freidin however, focuses solely on making the read/write control signals of different processors universal, while Geldman addresses a method of providing a flexible SCSI disk controller. While both references do mention

operability with both Intel and Motorola processors, neither specifically addresses a complete glueless processor interface.

Second, there is no evidence that the knowledge of one skilled in the art would provide for a suggestion to combine these references. In addition, glue logic has traditionally been the standard to tie unmatched bus protocols together. Here, however, the current invention specifies a bus interface system that does not necessarily need additional glue logic to connect the bus types.

Finally, the references' teachings themselves do not suggest or motivate any combination that would make the current inventive idea obvious, as detailed above.

For at least the reasons set forth above, the applicant submits that independent claims 1, 7, and 15 are in proper form for allowance.

Based at least in part upon their dependence from independent claims 1, 7 or 15, the applicant submits that claims 2, 3, 5, 6, 8, 9, 10, and 16 are believed to be in proper form for allowance as well.

Allowable Subject Matter

Claims 4, 13, 14, and 17-19 were objected to as being dependent upon a rejected base claim, but were indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

The applicant appreciates the examiner's acknowledgment of such allowable subject matter, and has amended claims 4, 13, and 17 to incorporate the elements of claims 1, 7 and 15 respectively.

CONCLUSION

In light of the above amendments and remarks, this application is now in condition for allowance. Claims 1-10 and 13-26 are currently pending. Early issuance of Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393. A Fee Transmittal is enclosed in duplicate for fee processing purposes.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

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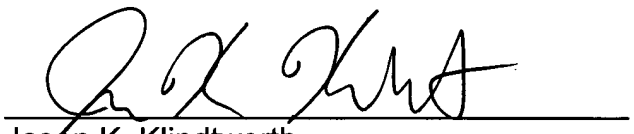

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